The invention can be used as part of a circuit or software instruction sequence design library. The invention can be included as part of a computer program that automatically generates efficient machines and methods for hardware circuitry and software instruction sequences.

An alternative embodiment of the invention has two or more multipliers with one or more multipliers using intermediate terms computed by one or more other multipliers. Several multipliers can compute intermediate terms to be shared with several other multipliers. Still another alternative embodiment of the invention has a multiplier capable of computing multiple outputs with shared computation of two or more outputs.

The description above contains many specific details relating to finite-precision numeric formats, representation elements, number values, computational complexity measures, discrete Fourier transforms, discrete cosine transforms, discrete sine transforms, inverse transforms, FFT techniques, hardware technologies, software technologies, and signal processing applications. These should not be construed as limiting the scope of the invention, but as illustrating some of the presently preferred embodiments of the invention. The scope of the invention should be determined by the appended claims and their legal equivalents, rather than by the examples given.